

Appl. No. 10/724,483
Amdt. Dated 04/26/2006
Reply to Office action of March 28, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) Method of forming different gate oxides on a semiconductor substrate, the substrate having a top surface, a first area and second area which is distinct from the first area, comprising:
 - forming a first gate oxide on the top surface of the substrate;
 - depositing a first layer of polysilicon over the first gate oxide;
 - forming a hard mask on top of the first layer of polysilicon;
 - forming a soft mask covering the first gate oxide, first layer of polysilicon and hard mask in the first area of the substrate;
 - removing the hard mask, the first layer of polysilicon and the first gate oxide in the second area of the substrate, leaving the second area exposed;
 - stripping the soft mask;
 - cleaning the exposed second area of the substrate;
 - growing a second gate oxide on the top surface of the substrate in the second area; and
 - removing the hard mask;
 - after removing the hard mask depositing a second layer of polysilicon in both the first and second areas of the substrate .
2. (canceled)
3. (currently amended) A method, according to claim 1, wherein:
 - the first ~~dielectric~~ gate oxide comprises a material selected from the group consisting of silicon dioxide (SiO₂), silicon oxynitride (SiON), silicon nitride (SiN) and high-k material.
4. (currently amended) A method, according to claim 1, wherein:

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- the first ~~dielectric~~ gate oxide has a thickness of approximately 5 - 25 Angstroms.
5. (currently amended) A method, according to claim 1, wherein:
the first layer of polysilicon has a thickness of approximately 20-500 Angstroms.
6. (currently amended) A method, according to claim 1, wherein:
the hard mask comprises a material selected from the group consisting of germanium (Ge), silicon germanium (SiGe), amorphous carbon, SiO₂, Si₃N₄, and other materials that are easy to remove from a silicon wafer without leaving a residue.
7. (Original) A method, according to claim 1, wherein:
the hard mask has a thickness of approximately 300-500 Angstroms.
8. (Original) A method, according to claim 1, further comprising:
choosing an initial thickness for the hard mask to ensure that after stripping the soft mask, a thickness of greater than approximately 15 Angstroms of hard mask material remains in place on-the substrate.
9. (Original) A method, according to claim 1, wherein:
the second gate oxide comprises a material selected from the group consisting of silicon dioxide (SiO₂), silicon oxynitride (SiON), silicon nitride (SiN) and high-k material.
10. (currently amended) A method, according to claim 1, wherein:
the second gate oxide is grown by a process selected from the group consisting of:
rapid thermal oxidation (RTO) in NO, N₂O, NH₃, O₂ (500-1100 degrees C);
plasma nitridation treatment on base oxide (25 - 800 degrees C); and
plasma oxidation; UV oxidation; and atomic layer deposition.
11. (currently amended) A method, according to claim 1, wherein:
during ~~growing~~ the step of growing the second gate oxide, a portion of the hard mask

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becomes oxidized; and

further comprising:

removing the oxidized portion of the hard mask using an etch that will remove the oxidized portion of the hard mask without affecting the second gate oxide.

12. (Original) A method, according to claim 1, wherein:
the first gate oxide is thinner than the second gate oxide.
13. (Original) A method, according to claim 1, wherein:
the first gate oxide comprises a high-k material.
14. (Original) A method, according to claim 1, wherein:
the second gate oxide has a composition that is different than a composition of the first gate oxide.
15. (currently amended) Method of forming gate oxides dielectrics on a semiconductor substrate, the substrate having a top surface, a first area and a second area which is distinct from the first area, comprising:
forming a first gate oxide dielectric on the top surface of the substrate;
next depositing a first layer of polysilicon over the first gate dielectric;
next protecting the first gate oxide dielectric from damage during subsequent processing steps by forming a sacrificial hard mask over a selected area of the first layer of polysilicon which is over the first gate oxide dielectric; and
then next forming a second gate oxide dielectric in the second area;
next removing the sacrificial hard mask; and
after removing the sacrificial hard mask, depositing a second layer of polysilicon over the second gate dielectric and over the first layer of polysilicon.
16. (canceled)
17. (canceled)

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- 18. (canceled)
- 19. (canceled)
- 20. (canceled)

Please enter the following:

- 21. (new) A method, according to claim 15, wherein:
the first gate dielectric comprises a material selected from the group consisting of silicon dioxide (SiO₂), silicon oxynitride (SiON), silicon nitride (SiN) and high-k material.
- 22. (new) A method, according to claim 15, wherein:
the second gate dielectric comprises a material selected from the group consisting of silicon dioxide (SiO₂), silicon oxynitride (SiON), silicon nitride (SiN) and high-k material.
- 23. (new) A method, according to claim 15, wherein:
the sacrificial hard mask comprises a material selected from the group consisting of germanium (Ge), silicon germanium (SiGe), amorphous carbon, SiO₂, Si₃N₄, and other materials that are easy to remove from a silicon wafer without leaving a residue.
- 24. (new) A method, according to claim 15, wherein:
the second gate dielectric is formed by a process selected from the group consisting of:
rapid thermal oxidation (RTO) in NO, N₂O, NH₃, O₂ (500-1100 degrees C);
plasma nitridation treatment on base oxide (25 - 800 degrees C); and
plasma oxidation; UV oxidation; and atomic layer deposition.
- 25. (new) A method, according to claim 15, wherein:
the first gate dielectric is thinner than the second gate dielectric.
- 26. (new) A method, according to claim 15, wherein:
the first gate dielectric comprises a high-k material.